Design for Testability in 3-Dimensional Assemblies

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Abstract

3DANN, a 3D mixed-mode multiple IC stacked processor capable of 1 TeraOPS, presented many novel problems related to testability. This paper will discuss the design process for 3DANN and the test features developed to overcome the 3D testability problems. Test structures and circuits were designed so that every component in each IC can be tested even when the stack is fully assembled which makes individual ICs are difficult to reach. Many of these problems are inherent in 3D stacking and must be solved.

1 Introduction

As we strive to implement more and more complex algorithms in hardware, this new hardware must also grow in complexity. First came mixed-mode ICs and processors, which were sufficient for simple problems. Image processing algorithms, however, regularly employ $O(n^4)$ computation with large sets of parallel data, which is impractical with 2D architectures. [1] The next step is hardware in three dimensions in order to accommodate size, power and processing requirements that 2D ICs can not satisfy. Designing an mixed-mode IC to be stacked in a 3D cube poses a new set of design problems and requirements. One must pay special attention to design for testability. Test structures and procedures have to be designed to be useful when the entire cube is assembled.

2 Test Structures for 3D

3D architectures must include test structures that can be accessed while the ICs are in a stack. In a stack, test structures such as internal test pads are physically blocked from access by the other ICs in the stack. All testing has to be done from the external I/O pads.

Conventional boundary-scan or memory read/write tests may be used for digital portions, but analog testing presents a different problem. Internal test structures and built-in self test must be designed so that each part of the signal path can be isolated and its inputs and outputs independently controlled and observed externally or via built-in test structures. Not only do isolation structures have to be built, but they must either be totally transparent to the signal path, or the signal path must be designed to compensate for the them.

3D stacking may also impose limitations on the number, location, and type of I/O pads available for use. If the IC is pad-limited, the design will have to assign more than one function per pad during testing. Examples include boundary scan outputs or internal state output for digital signals and arbitrary signal chain interruption for input/output on analog pads.

3 VIGILANTE and the 3DANN processor

VIGILANTE is an Automatic Target Recognition system that uses image-template correlation as a part of its core algorithm. It performs a convolution of sixty-four 64x64 8-bit digital templates with an incoming 256x256 image at video frame-rates or better. In convolutions alone, this equates to over 1 TeraOPS, a computation rate that is orders of magnitude greater than what sequential processors can do. To achieve that speed, JPL designed a mixed-mode processor called 3DANN. 3DANN takes in a 64x64 8-bit digital sub-window of an image and converts it to analog. 3DANN then performs four-quadrant multiplication of every element in the image and templates in parallel to compute sixty-four dot-products. The entire multiplication and accumulation is done using current-mode circuits [1].

3DANN consists of four distinct functional blocks, as illustrated in Figure 1. The digital input and control logic, the bias block, which sets the DAC's seed current, the image DAC array, and the multiplier section, which stores the templates digitally and contains all the hybrid multipliers. The internal logic of the cube is simple, and much of the functionality of the digital section of the cube is externally controlled. The cube is assembled by stacking and gluing sixty-four individual ICs together. Interconnect is accomplished by photo-lithography along one side of the cube. All analog and digital input and outputs are bussed together save one unique digital I/O pin per IC. The cube is then directly wire-bonded to support circuitry.

4 Test Structures and Procedures for 3DANN

Many test structures were designed and implemented for 3DANN. Test structures and procedures were chosen not only to satisfy testability in a stack, but were also chosen so that once one IC was tested, the same test hardware and procedures could be scaled by a factor

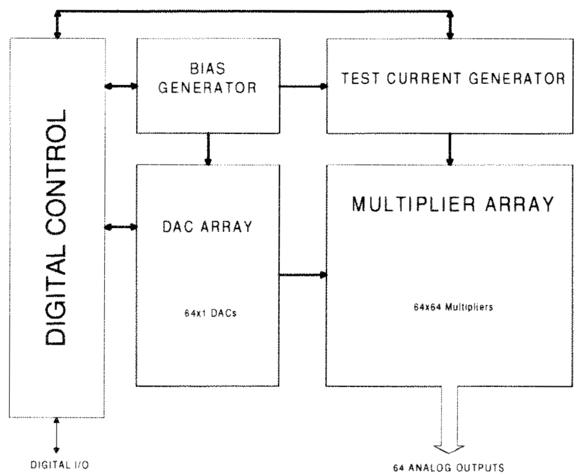

Figure 1: A simplified block diagram of the 3DANN Processor

of sixty-four to test the cube. Complicating this effort was the fact that the cube was I/O pad limited due to assembly requirements. The same pads used for I/O had to be used for test as well. Care had to be used when choosing which and how to multiplex normal I/O and test signals.

4.1 Digital

The digital section of the IC consists mainly of a large bi-directional shift register used to receive data which can then be directed to the various control registers, DAC values, multiplier values, and/or bias values. This shift register can also read data from every control register, DAC value, multiplier value, bias value as well the control logic's internal state, and output data back to the outside world on the same pin used for input. Every effort was made to make every writable value readable as well for 100% visibility.

Standard memory tests are used to test the digital section beginning with the most critical components and working towards least critical. First the shift register is tested. The register is filled with known values and then read back out and verified. Once the shift register is verified as operational, every memory location is verified.

4.2 Analog

The analog section of the IC is more complex and requires specialized circuits in order to fully test each section independent of the other sections in the signal chain. All these circuits must be fully controllable and have as little impact to circuit performance as possible.

Since the IC operates mainly in current-mode, a current must be generated if a single component is to be independently exercised. A setable Test Current Generator capable of generating anywhere from 50nA to 2mA was designed. Its output can be gated by an outside signal and can be routed to any section input available.

The bias block is simply tested by mirroring its output and routing the mirrored current directly to one of the main output stages. The DAC array received the same treatment. Each DAC output is mirrored and the mirrored current directly routed to its corresponding output stage.

The multiplier array has sixty-four main inputs from the DACs. Each input is multiplexed between the DAC output and the Test Current input. The multiplier array's output is also routed to the output stage directly.

Each output stage can be disabled so that no current is output onto the cube output bus. This is needed in order to be able to test each output independently of what the other outputs are doing. Each output stage takes its input multiplexed from all the sections mentioned previously.

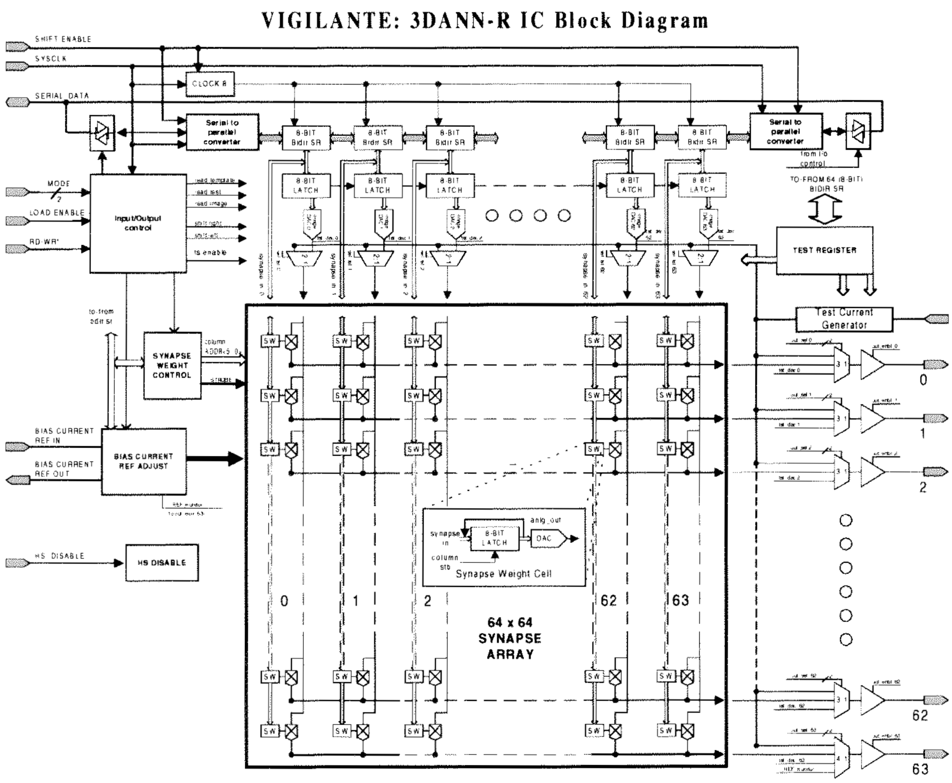

Figure 2: A detailed block diagram of the 3DANN Processor with test structures included.

A more detailed block diagram showing the relationship of all test structures can be found in Figure 2.

The procedure to test the Analog section is analagous to the digital procedure. The most critical parts are tested first followed by the least. The first section that is tested is the Bias block. It can be tested by selecting it for output on its assigned output pin. Various values are loaded into the bias block and the output is evaluated for functionality within specifications.

The next section to be tested is the Test Current Generator and output stages. All outputs are disabled and the test current generator is enabled with a known value. Each output mux is set to select the test current and then enabled one at a time. Each output is evaluated for functionality.

Next to be tested is the DAC array. The output mux is set to select the DAC mirror current and each DAC is run through standard DAC tests such as functionality, linearity, monotinicity, and accuracy.

Finally, the multiplier array is tested. The output mux is set to select the multiplier array and each multiplier input mux is set to take its input from the Test Current Generator. Each multiplier is then individually stepped through its inputs, then as a group, and then checked for cross-talk and/or shorting.

5 Conclusion

The 3DANN processor demonstrates that it is possible to design for test in projects with limited access to IC internals. The IC was designed and fabricated and all designed-in test structures were satisfactorily demonstrated. While each design may be different, all ICs can be designed to be tested from only its pads and in conjunction with the other ICs in the stack. Design for test has to approached with special consideration and care for 3D stacks.

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